Project ID # elt246

Implementation of WBG devices in circuits, circuit topology, system integration as well as SiC devices

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Overview

Timeline

- Project start: April 01, 2019
- Project end: March 31, 2024
- Percent Complete: 60%

Budget

- Total project funding: $ 1.5 M
- BP1 funding: $ 300 K
  BP2 funding: $ 300 K
  BP3 funding: $ 300

Barriers

- Commercial devices are not ready for insertion into a vehicle power train for long operational life.
- A comprehensive reliability study will be undertaken for currently available commercial devices and better devices will be designed.

Partners

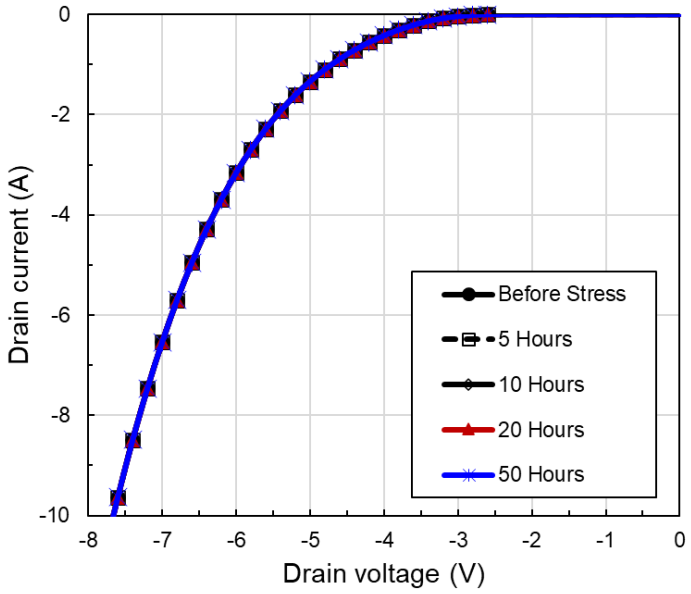
- Sandia National Laboratories
- SUNY POLYTECHNIC INSTITUTE,

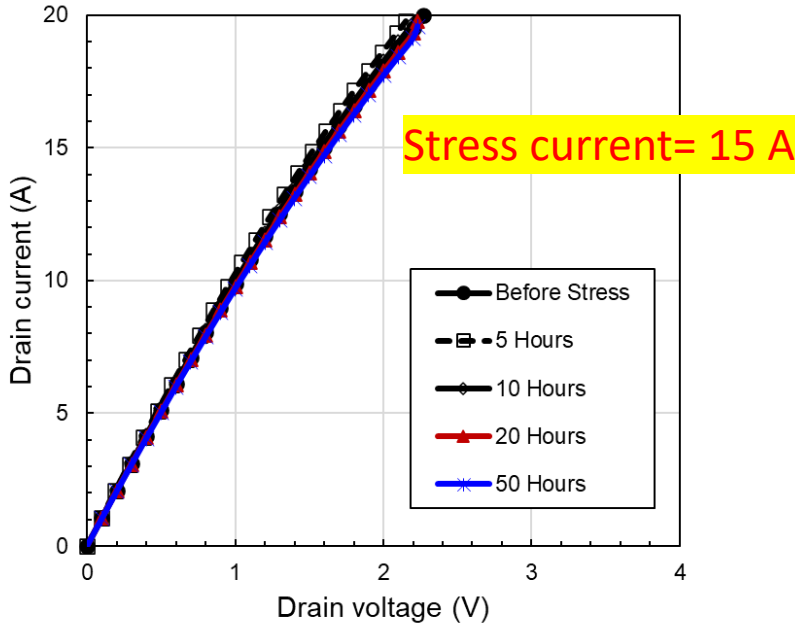
  Albany, NY

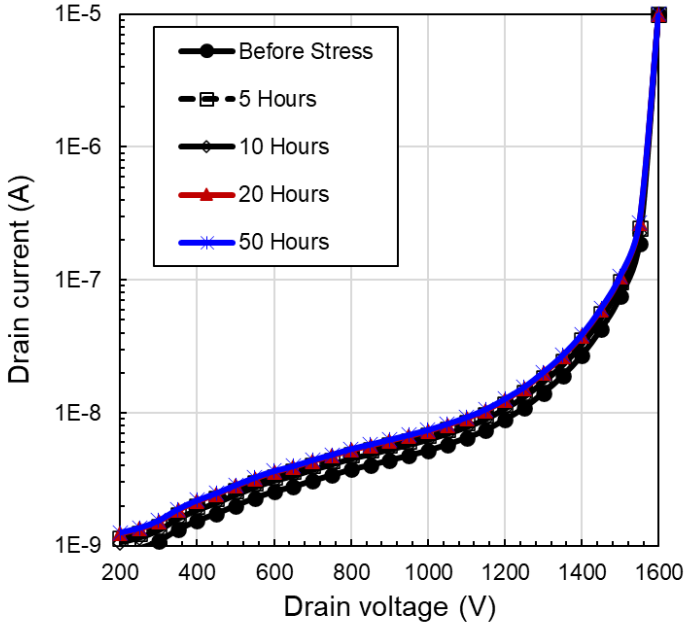
- **Project Objectives:**
  - –The advanced SiC MOSFETs are built every year by SUNY POLY.
  - –OSU is testing above MOSFETs as (1) stand-alone, (2) in a 10 kW inverter.

- **Deliverables so far:**
  - **–Room Temperature Implants can be used w/o body diode degradation for 1200 V MOSFETs. 30% cost reduction.**
  - **– 7 µs SCWT without any performance penalty. Commercial devices range from 2-4 µs.**
  - **–10 kVA inverter with 77 kVA/L and peak η of 98.8% has been developed to evaluate SiC MOSFETs from SUNY POLY.**

All tested Gen-2 devices with RT implants didn't show any body diode degradation

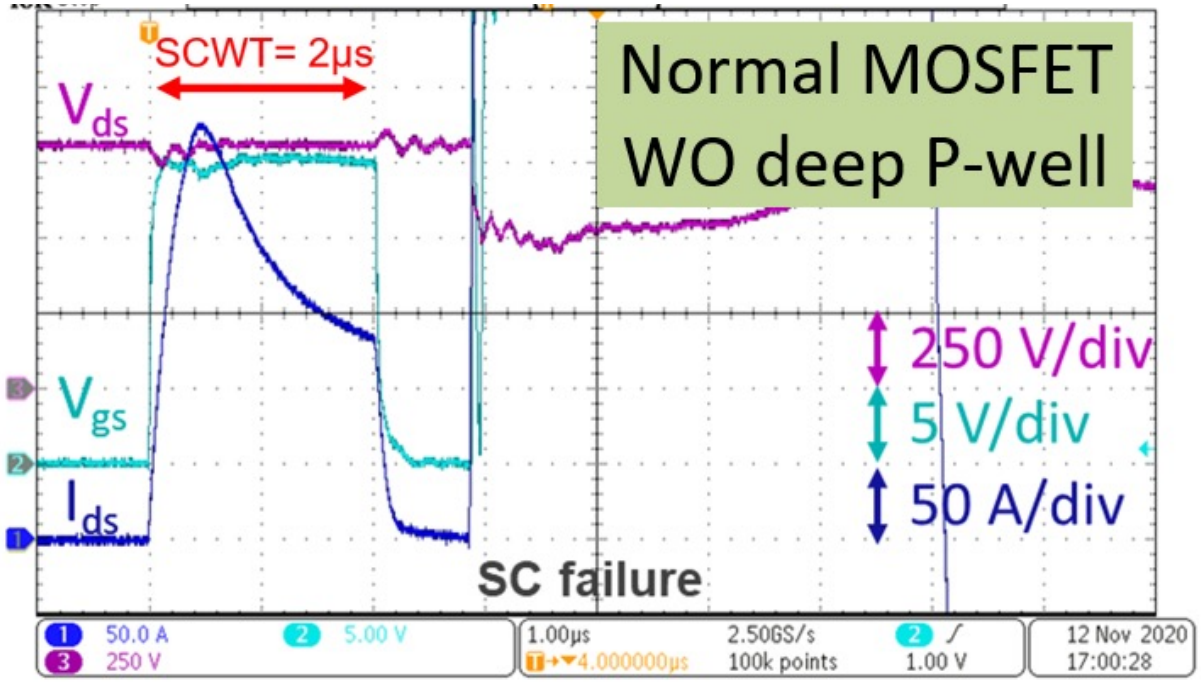




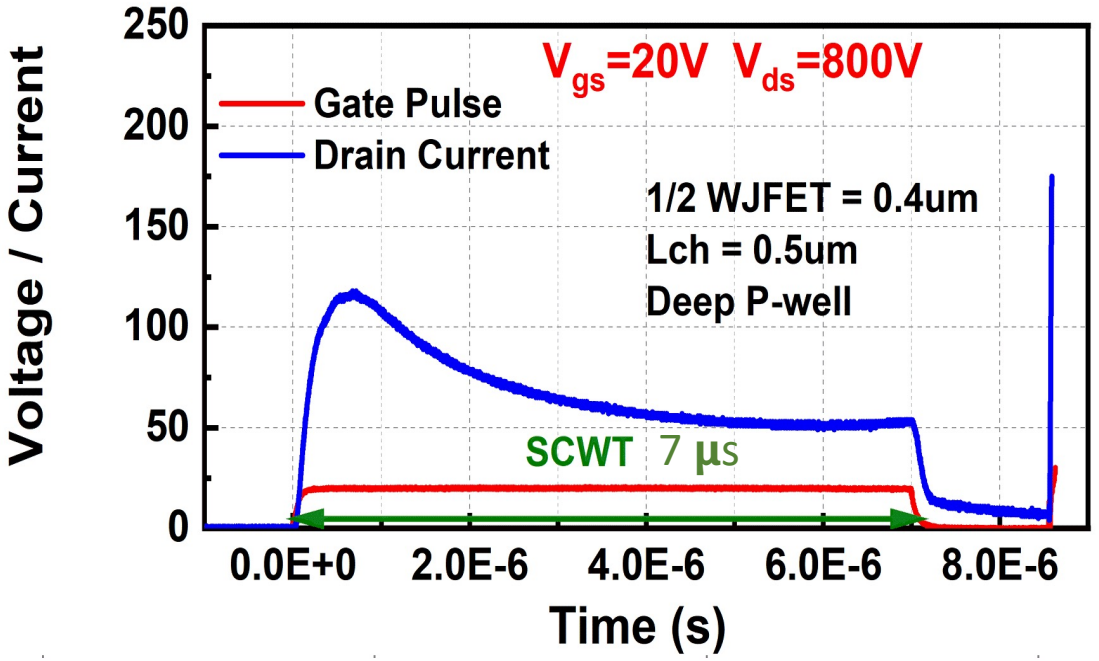


Room Temperature Implants can be used w/o body diode degradation for 1200 V MOSFETs – 30% cost savings

Short Circuit Withstand Time has been increased to 7 µs



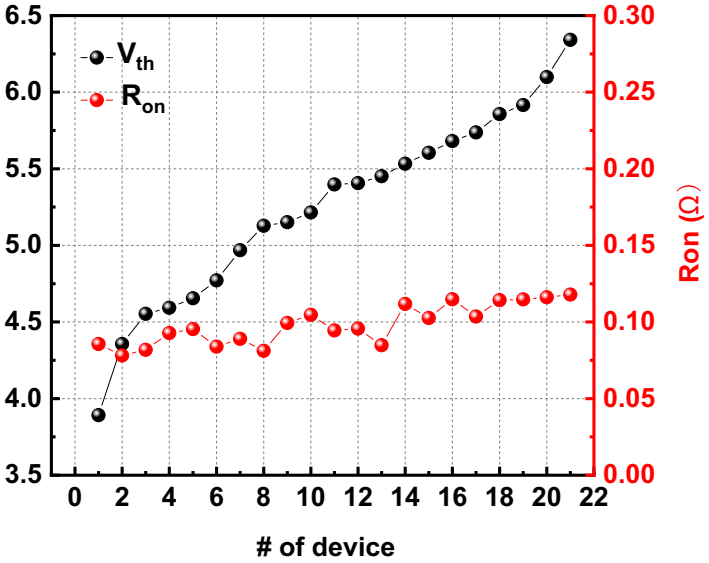
Gen-2 SUNY Poly MOSFETs with deep P-Well

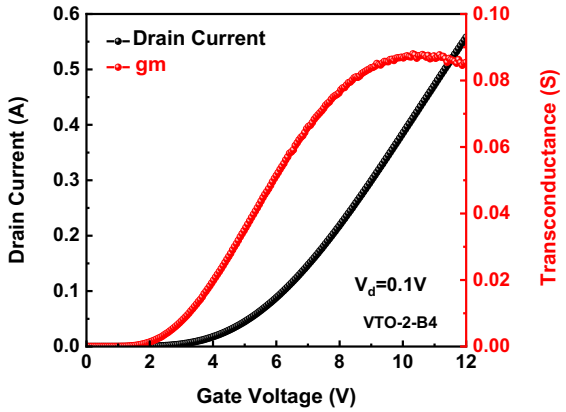


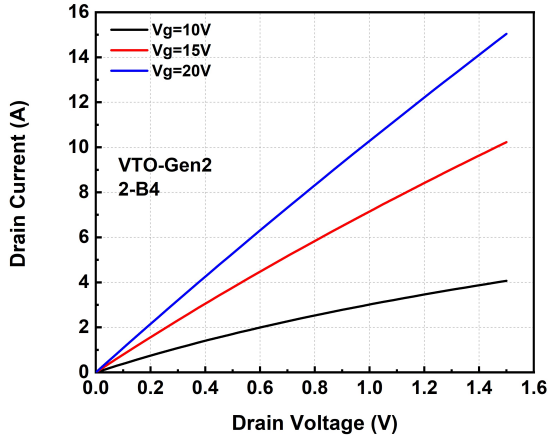
Deep p-well improves Short Circuit Withstand Time (SCWT) to 7 µs
This represents major technical breakthrough

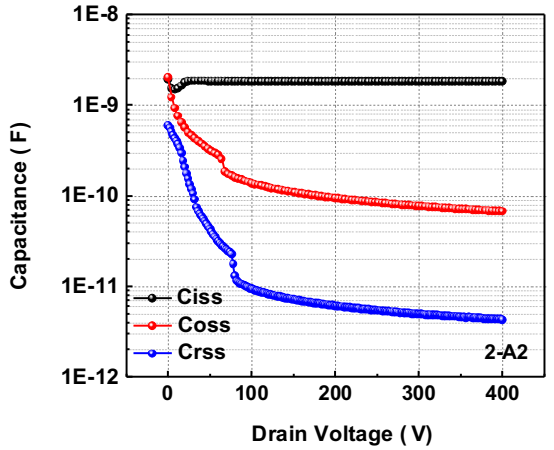
Technical Accomplishments and Progress

Device	#	Channel length (um)	1/2JFET width (um)	Vth (V)	Ron (Ω)	Ciss (F @ Vds=400V)	Coss (F @ Vds=400V)	Crss (F @ Vds=400V)
VTO-Gen2	VTO-2-A2	0.5	0.8	5.915868747	0.114765347	1.82063E-09	6.710E-11	4.30E-12
	VTO-2-A3	0.5	0.8	6.34166167	0.117879836	1.83182E-09	6.69000E-11	4.15E-12
	VTO-2-A5	0.5	0.8	6.098491768	0.116158045	1.81468E-09	8.63000E-10	3.79E-12
	VTO-2-B3	0.5	0.6	5.680990623	0.114809142	1.8496E-09	6.79000E-10	3.95E-12
	VTO-2-B4	0.5	0.6	5.604473233	0.102570975	1.79631E-09	6.64000E-11	3.12E-12
	VTO-2-B6	0.5	0.6	5.736885747	0.103584012	1.80539E-09	6.70000E-11	4.36E-12
	VTO-2-C2	0.5	0.4	5.214740832	0.104714557	1.77019E-09	6.60000E-11	1.77E-12
	VTO-2-D1	0.4	0.8	5.406413053	0.095683673	1.86967E-09	6.68000E-11	2.92E-12
	VTO-2-D3	0.4	0.8	4.968349064	0.089039924	1.80208E-09	6.7200E-11	5.04E-12
	VTO-2-D5	0.4	0.8	5.397467179	0.094473273	1.79094E-09	6.65000E-11	4.31E-12
	VTO-2-E1	0.4	0.4	4.654538971	0.095391822	1.73838E-09	6.60000E-11	1.82E-12
	VTO-2-E2	0.4	0.4	4.59305796	0.092768697	1.79652E-09	2.66000E-10	3.53E-13
	VTO-2-E3	0.4	0.4	5.151567313	0.099352957	1.76018E-09	6.51000E-11	9.13E-13
	VTO-2-F1	0.3	0.8	5.451831753	0.084823971	1.7998E-09	6.68000E-11	3.79E-12
	VTO-2-F2	0.3	0.8	4.553473947	0.081867725	1.78954E-09	9.88000E-11	4.90E-12
	VTO-2-F3	0.3	0.8	4.355900022	0.078139205	1.80895E-09	6.87000E-11	4.75E-12
	VTO-2-G1	0.3	0.4	3.892037372	0.085608133	1.70461E-09	6.57000E-11	1.77E-12





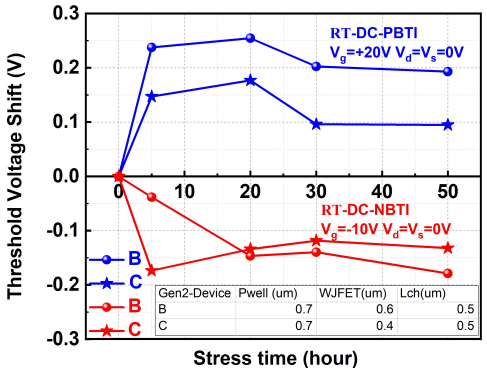




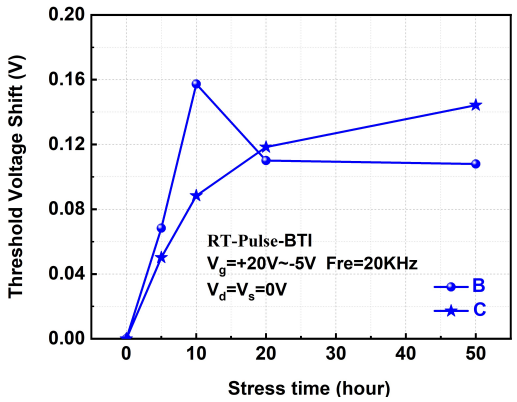
Many Gen-2 MOSFETs from SUNY POLY have been evaluated by OSU

SUNY POLY MOSFETS compare well with commercial devices

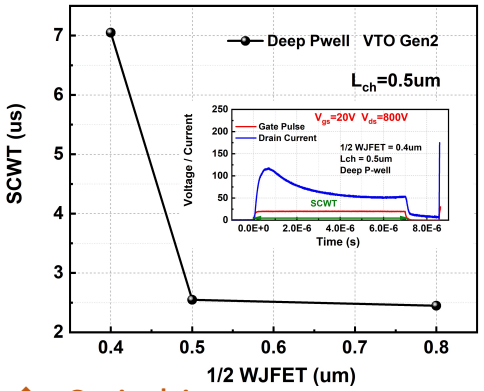
Threshold voltage instability- BTI measurement

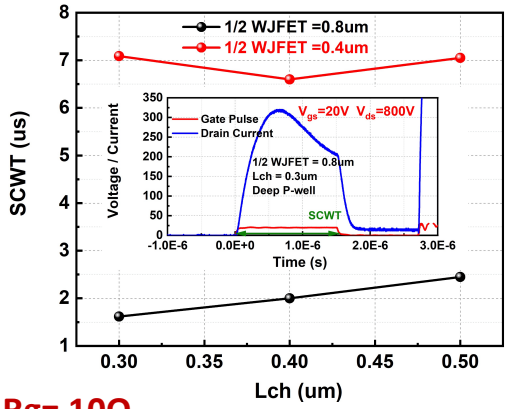


Gen2-Device	Pwell (um)	WJFET(um)	Lch(um)
B	0.7	0.6	0.5
C	0.7	0.4	0.5



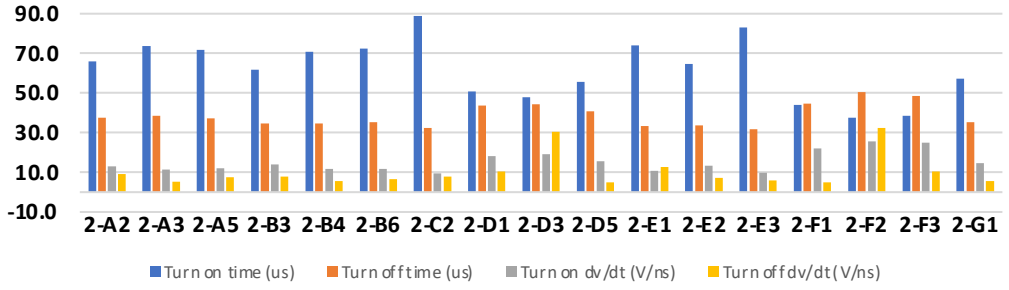
Short circuit measurement





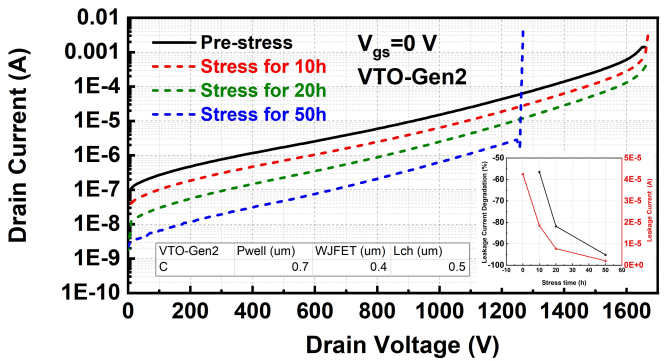
Switching measurement

Rg= 10Ω

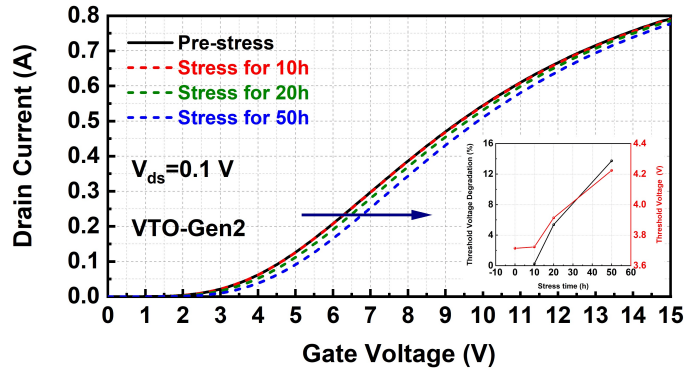


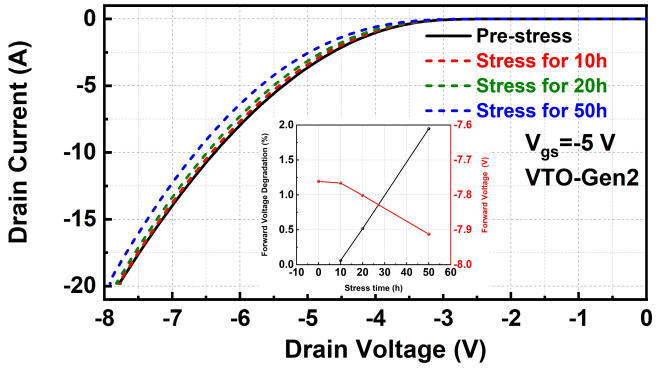
Body diode degradation measurement

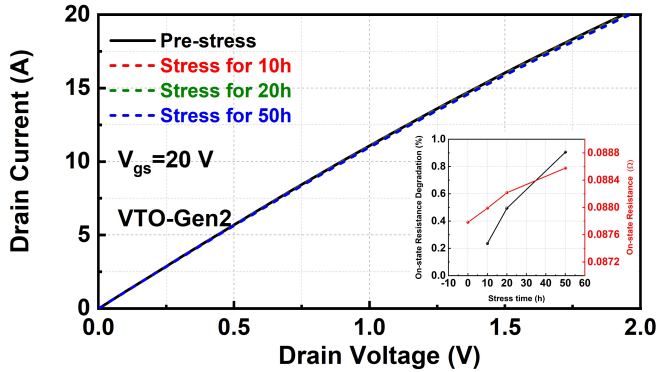
Vg= -5V Current stress = 15A



VTO-Gen2	Pwell (um)	WJFET (um)	Lch (um)
C	0.7	0.4	0.5

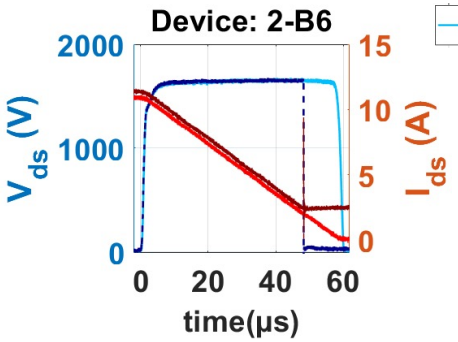


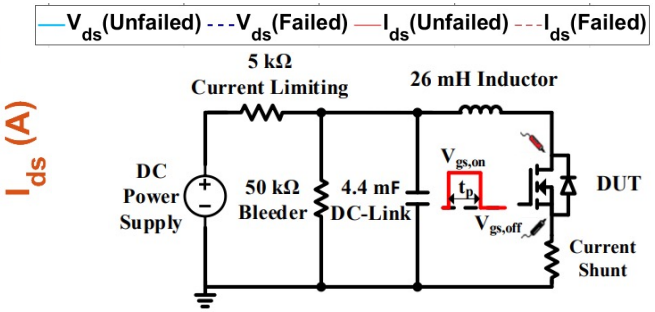




Avalanche measurement

Device	1/2WJFET(um)	Lch (um)
2-A#	0.8	0.5
2-B#	0.6	0.5
2-C#	0.4	0.5
2-D#	0.8	0.4
2-E#	0.4	0.4
2-F#	0.8	0.3
2-G#	0.4	0.3





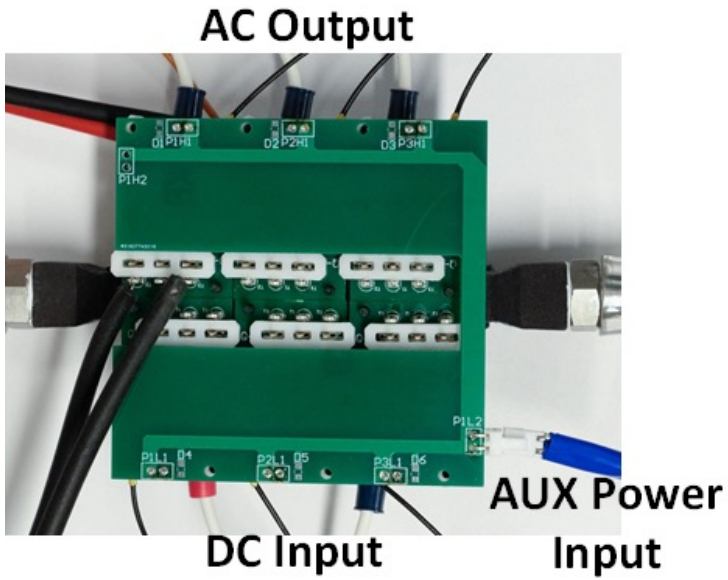
Gen-2 devices from SUNY POLY evaluated with Inverter-2 - 11 kVA, average efficiency = 98.5%, power density = 77 kVA/L

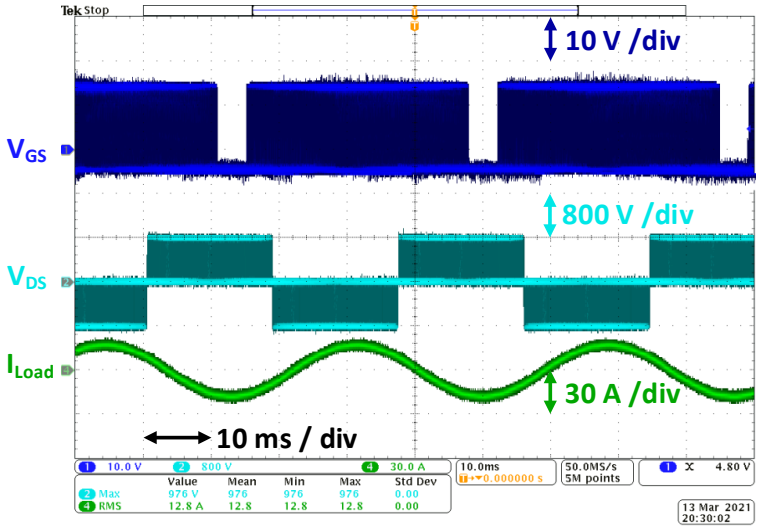
Gen-2 Device Switching Performance Evaluation:

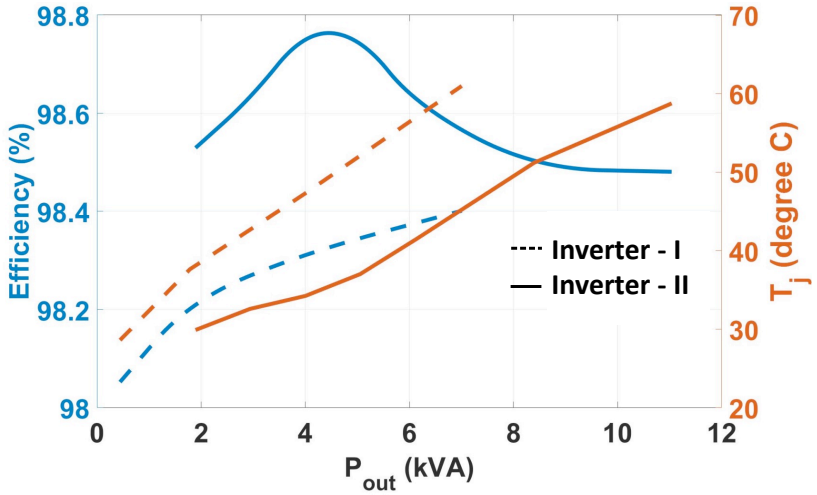
Device	20 Ohms R_G	
	Switch on (μJ)	Switch off (μJ)
4-A1	427.78	257.72
4-A2	411.70	216.97
4-N2	420.55	249.65
4-N3	446.06	256.19
4-O1	528.52	283.03
4-O3	534.20	282.51
4-S2	486.50	274.48

Inverter-2 Operation Condition

Output Power	11 kVA
Estimated T_J	58.7 ℃
Efficiency	98.5%
Operation Duration	10 Min

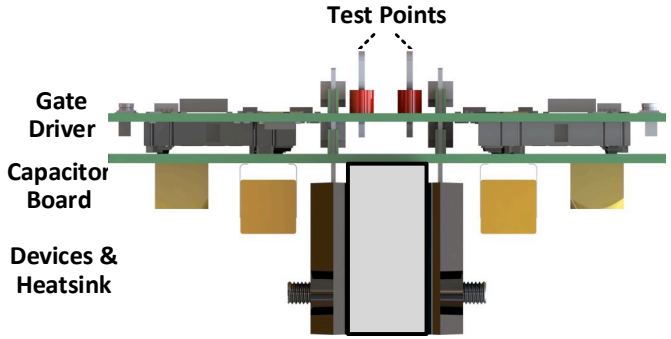




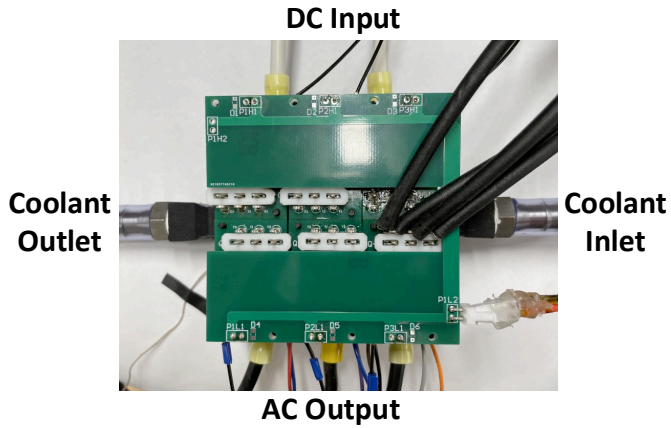


Inverter-3 built and debugged: 11 kVA, average efficiency = 98.5%, power density = 77 kVA/L

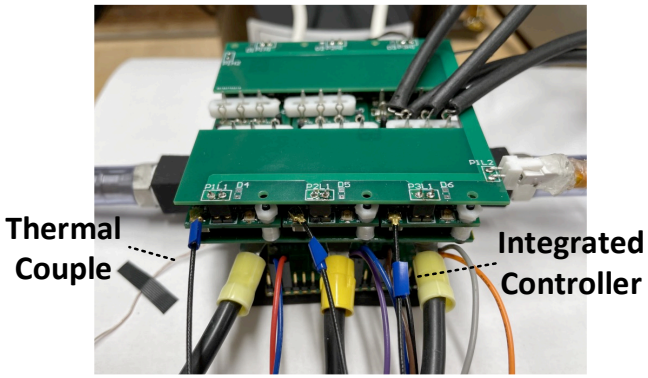
Gen-3 Inverter Build with Gen-2 Devices:



Inverter-3 Power Stage and Gate Driver



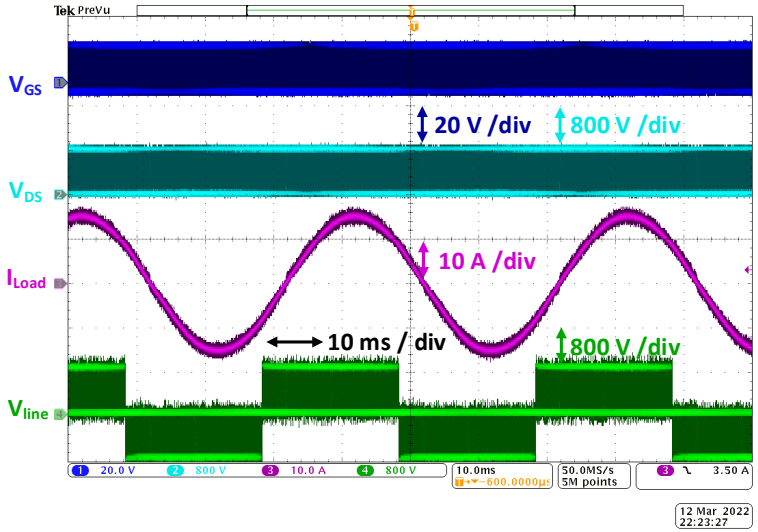
Inverter-3 Test Setup Top View

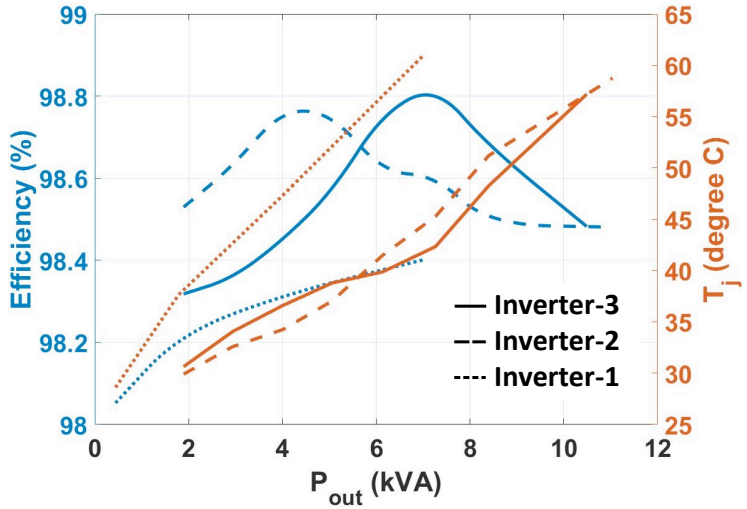


Inverter-3 Test Setup Side View

Inverter-3 Operation Condition

Output Power	10.5 kVA
Estimated T_J	57.2 ℃
Efficiency	98.5%
Operation Duration	10 Min





Proposed Future Research

Stand-alone device failure mechanism tests on Gen-3 devices:

Body diode stability, threshold voltage stability, short circuit time and avalanche energy tests will be evaluated

Gen-3 devices will be evaluated with Inverter-3:

Gen-2 devices fully will be evaluated with the Inverter-3 at accelerated temperature and power cycles

Summary

- **Room Temperature Implants can be used w/o body diode degradation for 1200 V MOSFETs. 30% cost reduction.**
- **Short Circuit withstand time has been increased to 7 us. 10 us can be achieved in future.**
- Newly designed 10 kVA three-phase inverter-2 delivers higher power density, better reliability and efficiency.
- Inverter-2 is stressed under full load, the performance of new designed cooling system is improved.
- Inverter-3 is ready.